IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Seri	al No	 		09/653,149
Pare		 		August 31, 2000
Inventor		 	Garo J.	Derderian, et al
Assignee		 	Micron	Technology, Inc
Group Art Unit .		 	• • • • • • • • • • • • • • • • • • •	2818
Examiner		 		T. Lee
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Title: Capacitor Fabrication Methods Including Forming a Conductive Layer

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

To:

Commissioner for Patents

PO Box 1450 Art Unit 2818

Alexandria, VA 22313-1450

From:

James E. Lake (Tel. 509-624-4276; Fax 509-838-3424)

Wells St. John P.S.

601 W. First Avenue, Suite 1300 Spokane, WA 99201-3828

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art. Citation of these references is respectfully requested.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Respectfully submitted,

Dated:	26 Jan 2004	ву: <u>250</u> 0	Q 501		
		James E. Lake Reg. No. 44,854			

Form PTO-1449				DEPARTMENT OF COMMERCE ATTY. DOCKET NO. MI22-1330			NO.	SERIAL NO. 09/653,149			
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U.S. PATENT DOCUMENTS											
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